Claims

[c1] 1. A bump layout on a driver integrated chip (IC) having an active region, wherein the bumps are positioned in an array format over the active region.

[c2] 2. The bump layout of claim 1, wherein the active region further includes a plurality of circuit blocks.

[c3] 3. The bump layout of claim 2, wherein the circuit blocks are laid down in the bump space between neighboring bumps.

[c4] 4. The bump layout of claim 1, wherein the bumps are positioned in vertically aligned rows.

[c5] 5. The bump layout of claim 1, wherein the bumps are positioned in alternatively staggered rows.

[c6] 6. The bump layout of claim 1, wherein the bumps are positioned in vertically aligned rows on part of the active region and in alternatively staggered rows on another part of the active region.

[c7] 7. A bump layout on a driver integrated circuit (IC), comprising:
a narrow and long driver IC package having an active region, wherein the package has a first short side, a second short side, a first long side and a second long side; and
a plurality of bumps over the active region close to the first long side and the second long side and over some other part of the active region so that the active region is divided into a plurality of circuit blocks.

[c8] 8. The bump layout of claim 7, wherein a plurality of dummy bumps are also formed over active regions close to the first short side and the second short side of the driver IC package.

[c9] 9. The bump layout of claim 7, wherein the bumps close to the first long side are positioned in a vertically aligned grid format.

[c10] 10. The bump layout of claim 7, wherein the bumps close to the first long side are positioned in alternatively staggered row format.

[c11] 11. The bump layout of claim 7, wherein the bumps close to the second long side are positioned in a vertically aligned grid format.

[c12] 12. The bump layout of claim 7, wherein the bumps close to the second long side are positioned in an alternatively staggered row format.

[c13] 13. The bump layout of claim 7, wherein the circuit blocks are electrically connected by circuit lines.